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App Serial 10/757,187**PATENT****IBM Docket No. RPS920030036US1****Amendments to the Claims:**

- 1 1. (Original) A parallel pattern detection engine (PPDE) integrated circuit (IC) for
2 detecting one or more patterns in a sequence of input data comprising:
3 an input/output (I/O) interface for coupling data into and out of the PPDE;
4 M processing units (PUs), each of the M PUs having compare circuitry for
5 comparing each of the sequence of input data to a pattern stored in each of the M PUs and
6 generating a compare output, wherein an address pointer selecting the pattern in each of
7 the M PUs is modified in response to a logic state of the compare output and an operation
8 code stored with the pattern;
9 an input bus for coupling the sequence of input data to each of the M PUs in parallel;
10 an output bus coupled to the I/O interface for sending output data to the I/O interface;
11 control circuitry coupled to the I/O interface and coupling control data on a control
12 data bus and identification (ID) on an ID bus to each of the M processing units;
13 ID selection circuitry for selecting a match ID from ID data identifying the M PUs in
14 response to a pattern match signal and match mode data, wherein the match ID and match
15 data corresponding to the match ID are saved in a temporary register as the output data;
16 and
17 cascade circuitry coupled from each of the M PUs to one or more adjacent PUs
18 within the M PUs for selectively coupling chain data between one or more groups of two or
19 more adjacent PUs selected from the M PUs in response to the control data.

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- 1 2. (Original) The PPDE of claim 1 further comprising an input buffer coupled to the
2 I/O interface for receiving and writing input data as parallel data at a write address.
- 1 3. (Original) The PPDE of claim 2 further comprising a multiplexer coupled to the
2 input bus and the input buffer for sequentially coupling single data from the input buffer data
3 to the input bus, wherein parallel data are selected using a read address.
- 1 4. (Original) The PPDE of claim 1 further comprising an output buffer coupled to the
2 output bus and to the temporary register for receiving and writing output data to the output
3 buffer at a write address and coupling output data to the output bus corresponding to a
4 read address.
- 1 5. (Original) The PPDE of claim 1, wherein each of M processing units (PUs) has an
2 ID register for storing a unique ID sent from the control circuitry.
- 1 6. (Original) The PPDE of claim 1, wherein each of M processing units (PUs) has a
2 control register for storing the match mode data, wherein the match mode data determines
3 criteria for generating the match signal and the match data.
- 1 7. (Original) The PPDE of claim 1, wherein each of the M PUs has a memory register
2 array for storing a sequence of the pattern and corresponding operation codes addressed
3 by an address register indexed by the address pointer.

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1 8. (Original) The PPDE of claim 1, wherein the cascade circuitry enables the stored
2 patterns of two or more PUs to be chained together as a single pattern using the chain
3 data.

1 9. (Original) The PPDE of claim 9, wherein the chain data inhibits indexing the pointer
2 of one PU until an adjacent PU coupled with the cascade circuitry has compared a last
3 pattern to an input data.

1 10. (Original) The PPDE of claim 1, wherein the compare circuitry in each of the M
2 PUs completes a compare of an input data to a selected pattern and generates a compare
3 output and modifies the address pointer in the same cycle of a clock signal.

1 11. (Original) The PPDE of claim 1, wherein the match mode data for each of the M
2 PUs sets a match mode comprising:

3 an exact match mode, wherein a pattern match indicates that the sequence of
4 pattern matches a sequence of input data exactly,

5 a longest match mode wherein a pattern match indicates that a particular sequence
6 of pattern corresponding to the match ID has the largest number of data in a sequence that
7 compared to a sequence of data in the sequence of input data wherein the match data
8 indicates the value of the largest number;

9 a maximum match mode, wherein a pattern match indicates that a particular
10 sequence of pattern bytes corresponding to the match ID has the largest number of data
11 that compared in a broken sequence that compared to a broken sequence of input data,
12 wherein the match data indicates the value of the largest number; and

13 a fuzzy match mode, wherein a pattern match indicates that a particular sequence
14 of pattern corresponding to the match ID has the closet match to the sequence of input data
15 as determined by a distance value, wherein the match data indicates the distance value.

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1 12. (Original) The PPDE of claim 1, wherein the operation codes are selected from a
2 set of operation codes comprising:
3 a match operation code indicating that the address pointer is incremented if the
4 compare output is a logic one and the address pointer is reloaded to its initial value if the
5 compare output is a logic zero;
6 an inverse operation code indicating that the address pointer is to be incremented
7 if the compare output is a logic zero and the address pointer is reloaded to its initial value
8 if the compare output is a logic one;
9 a wildcard operation code indicating that the address pointer is incremented if the
10 compare output is a logic zero or a logic one;
11 a multiple wild card operation code indicating that the address pointer is to be held
12 if the compare output is a logic zero otherwise the address pointer is incremented; and
13 a last operation code indicating that the address pointer is frozen until the matching
14 process receives a reset if the compare output is a logic one and the address pointer is
15 reloaded to its initial value if the compare output is a logic zero.

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1 13. (Original) The PPDE of claim 1, wherein bits of the selected pattern are masked
2 by a mask data stored in a mask register when the selected pattern is compared to an
3 input data, the mask data indicating which bits of the selected pattern are not compared.

1 14. (Original) A method of determining if any of N sequences of pattern occurs within
2 a sequence of input data using a parallel pattern detection engine (PPDE) comprising the
3 steps of:

4 a) loading the N sequences of pattern into M processing units (PUs), each of the M
5 PUs having compare circuitry for comparing each of the sequence of input data, in parallel,
6 to a selected pattern in each of the N sequences of pattern stored in the M PUs;

7 b) loading identification (ID) data into each of the M PUs, wherein the ID data
8 determines an ID for each of the M PUs;

9 c) loading match mode data into each of the M PUs setting criteria for determining
10 when conditions have been met for indicating that one of the N sequences of pattern has
11 been detected in the sequence of input data;

12 d) coupling a first input data in parallel to each of the M PUs;

13 e) comparing the first input data to the selected pattern determined by an address
14 pointer in each of the M PUs and generating a compare output in each of the M PUs within
15 a same clock cycle;

16 f) modifying the value of the address pointer in each of the M PUs in response to a
17 logic state of the corresponding compare output and an operation code stored with the
18 selected pattern in each of the M PUs;

19 g) selecting a match ID from the ID data in response to a pattern match signal
20 indicating one of the N sequences of pattern has been detected;

21 h) storing the match ID and match data corresponding to the match ID; and

22 i) repeating steps (a-g) until a last input data of the sequence of input data has been
23 compared.

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1 15. (Original) The method of claim 14, wherein cascade circuitry is coupled from each
2 of the M PUs to one or more adjacent PUs within the M PUs for selectively coupling chain
3 data between two or more adjacent PUs selected from the M PUs in response to control
4 data loaded into the two or more adjacent PUs.

1 16. (Original) The method of claim 14, one of the N sequences of pattern are
2 partitioned and loaded into the two or more M PUs.

1 17. (Original) The method of claim 14, wherein each of M processing units (PUs) has
2 a control register for storing the match mode data, wherein the match mode data
3 determines criteria for generating the match signal and the match data.

1 18. (Original) The method of claim 17, wherein each of the M PUs has a memory
2 register array for storing a sequence of the pattern and corresponding operation codes
3 addressed by an address register indexed by the address pointer.

1 19. (Original) The method of claim 15, wherein the cascade circuitry enables the stored
2 patterns of two or more PUs to be chained together as a single pattern using the chain
3 data.

1 20. (Original) The method of claim 19, wherein the chain data inhibits indexing the
2 pointer of one PU until an adjacent PU coupled with the cascade circuitry has compared
3 a last pattern to an input data.

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1 21. (Original) The method of claim 14, wherein compare circuitry in each of the M PUs
2 completes a compare of an input data to a selected pattern and generates a compare
3 output and modifies the address pointer in the same cycle of a clock signal.

1 22. (Original) The method of claim 14, wherein the match mode data for each of the
2 M PUs sets a match mode comprising:

3 an exact match mode, wherein a pattern match indicates that the sequence of
4 pattern matches a sequence of input data exactly;

5 a longest match mode wherein a pattern match indicates that a particular sequence
6 of pattern corresponding to the match ID has the largest number of data in a sequence that
7 compared to a sequence of data in the sequence of input data wherein the match data
8 indicates the value of the largest number;

9 a maximum match mode, wherein a pattern match indicates that a particular
10 sequence of pattern corresponding to the match ID has the largest number of data that
11 compared to a broken sequence of input data, wherein the match data indicates the value
12 of the largest number;

13 a fuzzy match mode, wherein a pattern match indicates that a particular sequence
14 of pattern corresponding to the match ID has the closet match to the sequence of input data
15 as determined by a distance value, wherein the match data indicates the distance value.

1 23. (Original) The method of claim 18, wherein the operation codes are selected from
2 a set of operation codes comprising:

3 a match operation code indicating that the address pointer is incremented if the
4 compare output is a logic one and the address pointer is reloaded to its initial value if the
5 compare output is a logic zero;

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6 an inverse operation code indicating that the address pointer is to be incremented
7 if the compare output is a logic zero and the address pointer is reloaded to its initial value
8 if the compare output is a logic one;
9 a wildcard operation code indicating that the address pointer is incremented if the
10 compare output is a logic zero or a logic one;
11 a multiple wildcard operation code indicating that the address pointer is to be held
12 if the compare output is a logic zero otherwise the address pointer is incremented; and
13 a last operation code indicating that the address pointer is frozen until the matching
14 process receives a reset if the compare output is a logic one and the address pointer is
15 reloaded to its initial value if the compare output is a logic zero.

1 24. (Original) A data processing system comprising:

2 a central processing unit (CPU);
3 a random access memory (RAM);
4 one or more parallel pattern detection engines (PPDEs); and
5 a bus coupling the CPU, RAM, and the one or more PPDEs, wherein each of the
6 PPDEs has an input/output (I/O) interface for coupling data into and out of the PPDE;
7 M processing units (PUs), each of the M PUs having compare circuitry for
8 comparing each of the sequence of input data to a pattern stored in each of the M PUs and
9 generating a compare output, wherein an address pointer selecting the pattern data in
10 each of the M PUs is modified in response to a logic state of the compare output and an
11 operation code stored with the pattern data;
12 an input bus for coupling the sequence of input data to each of the M PUs in parallel;
13 an output bus coupled to the I/O interface for sending output data to the I/O interface;
14 control circuitry coupled to the I/O interface and coupling control data on a control
15 data bus and identification (ID) on an ID bus to each of the M processing units;
16 ID selection circuitry for selecting a match ID from ID data identifying the M PUs in
17 response to a pattern match signal and match mode data, wherein the match ID and match

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18 data corresponding to the match ID are saved in a temporary register as the output data;
19 and

20 cascade circuitry coupled from each of the M PUs to one or more adjacent PUs
21 within the M PUs for selectively coupling chain data between one or more groups of two or
22 more adjacent PUs selected from the M PUs in response to the control data.

1 25. (Original) The data processing system of claim 24, wherein each of M processing
2 units (PUs) has an ID register for storing a unique ID sent from the control circuitry.

1 26. (Original) The data processing system of claim 24, wherein each of the M PUs has
2 a memory register array for storing a sequence of the pattern and corresponding operation
3 codes addressed by an address register indexed by the address pointer.

1 27. (Original) The data processing system of claim 24, wherein the cascade circuitry
2 enables the stored patterns of two or more PUs to be chained together as a single pattern
3 using the chain data.

1 28. (Original) The data processing system of claim 27, wherein the chain data inhibits
2 indexing the pointer of one PU until an adjacent PU coupled with the cascade circuitry has
3 compared a last pattern to an input data.

1 29. (Original) The data processing system of claim 24, wherein the compare circuitry
2 in each of the M PUs completes a compare of an input data to a selected pattern and
3 generates a compare output and modifies the address pointer in the same cycle of a clock
4 signal.

1 30. (Original) The data processing system of claim 24, wherein the match mode data
2 for each of the M PUs sets a match mode comprising:

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3 an exact match mode, wherein a pattern match indicates that the sequence of
4 pattern matches a sequence of input data exactly;

5 a longest match mode wherein a pattern match indicates that a particular sequence
6 of pattern corresponding to the match ID has the largest number of data in a sequence that
7 compared to a sequence of data in the sequence of input data wherein the match data
8 indicates the value of the largest number;

9 a maximum match mode, wherein a pattern match indicates that a particular
10 sequence of pattern corresponding to the match ID has the largest number of data that
11 compared to a broken sequence of input data, wherein the match data indicates the value
12 of the largest number; and

13 a fuzzy match mode, wherein a pattern match indicates that a particular sequence
14 of pattern corresponding to the match ID has the closet match to the sequence of input data
15 as determined by a distance value, wherein the match data indicates the distance value.

1 31. (Original) The data processing system of claim 30, wherein the operation codes
2 are selected from a set of operation codes comprising:

3 a match operation code indicating that the address pointer is incremented if the
4 compare output is a logic one and the address pointer is reloaded to its initial value if the
5 compare output is a logic zero;

6 an inverse operation code indicating that the address pointer is to be incremented
7 if the compare output is a logic zero and the address pointer is reloaded to its initial value
8 if the compare output is a logic one;

9 a wildcard operation code indicating that the address pointer is incremented if the
10 compare output is a logic zero or a logic one;

11 a multiple wildcard operation code indicating that the address pointer is to be held
12 if the compare output is a logic zero otherwise the address pointer is incremented; and

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13 a last operation code indicating that the address pointer is frozen until the matching
14 process receives a reset if the compare output is a logic one and the address pointer is
15 reloaded to its initial value if the compare output is a logic zero.

1 32. (Original) The data processing system of claim 30, wherein bits of the selected
2 pattern are masked by a mask data stored in a mask register when the selected pattern
3 is compared to an input data, the mask data indicating which bits of the selected pattern
4 are not compared.

1 33. (New) A method to recognize objects comprising:
2 providing a database of patterns representative of objects to be recognized;
3 storing an operation code with predefined sector of said database;
4 generating a data stream representative of unknown objects;
5 providing an address pointer to select patterns in said database;
6 correlating a pattern selected with a block of data from said data stream; and
7 generating a status signal based upon result of the correlation and the operation
8 code stored with the selected pattern.

1 34. (New) The method of claim 33 wherein correlation includes comparing the block
2 of data from the data stream with the pattern selected from said database of patterns.

1 35. (New) The method of claim 33 wherein predefined sector includes eight bits.

1 36. (New) The method of claim 33 wherein a selected block of data includes eight bits.

1 37. (New) The method of claim 33 wherein said status signal, indicating unknown
2 object identified, is being generated only if relationship between the data from said
3 data stream and selected pattern is consistent with operation code stored with said

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4 selected pattern.

1 38. (New) The method of claim 33 wherein said status signal, indicating unknown
2 object not identified, is being generated only if relationship between the data from
3 said data stream and the selected pattern is inconsistent with the operation code
4 stored with said selected pattern.

1 39. (New) The method of claim 33 further including selectively modifying the address
2 pointer in response to results of said correlation and the operation code stored with
3 the selected pattern.

1 40. (New) The method of claim 33 wherein the objects include digitized representation
2 of faces.

41. (New) The method of claim 33 or 34 wherein the block of data includes eight bits.

1 42. (New) A device comprising:
2 a memory;
3 a database of patterns stored in said memory;
4 a plurality of operation codes, with each one of said plurality of operation codes
5 being associated with selected pattern stored in said memory;
6 a register for storing a sequence of input data;
7 a pointer to select patterns in said memory; and
8 a controller correlating data from said register with selected pattern from said
9 database and issuing a status signal based upon result of the correlation and the operation
10 code stored with said selected pattern.